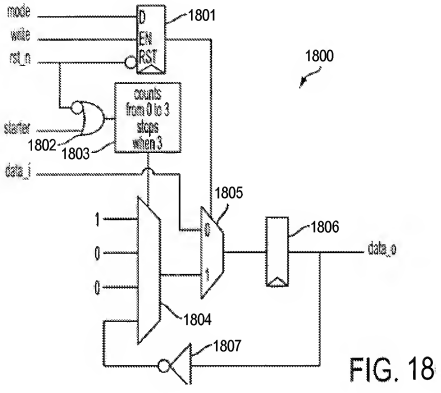
mode
write
rst_n
D
EN
RST
1801
1800
counts from 0 to 3 stops when 3
starter
1802
1803
data_i
1805
1
0
0
0
1
1806
data_o
1804
1807

FIG. 18

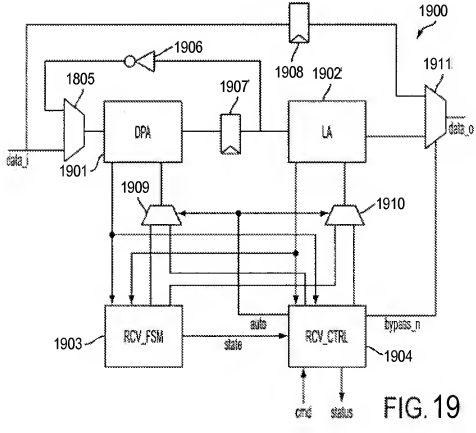
1900
1906
1908
1902
1911
1805
1907
DPA
LA
data_o
data_i
1901
1909
1910
RCV_FSM
auto
state
RCV_CTRL
bypass_n
1903
1904
cmd
status

FIG. 19

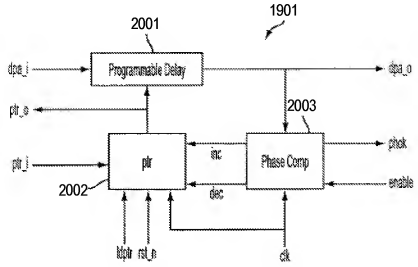

FIG. 20

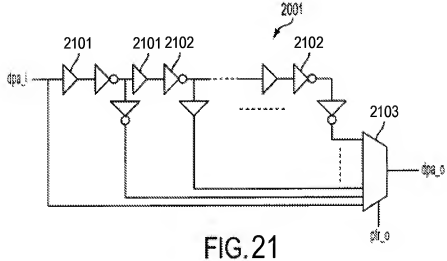

FIG. 21

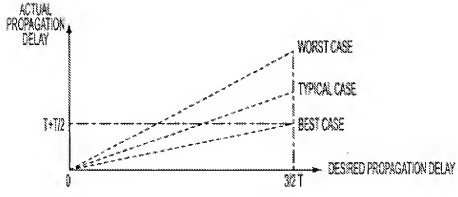

FIG. 22

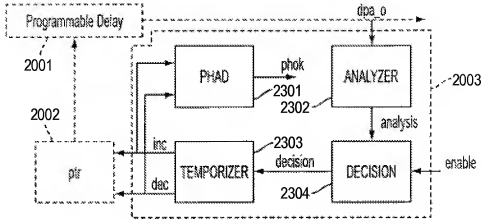

FIG. 23

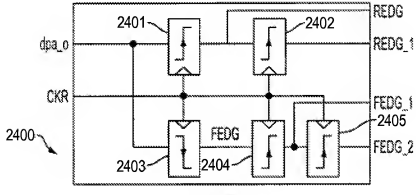

FIG. 24

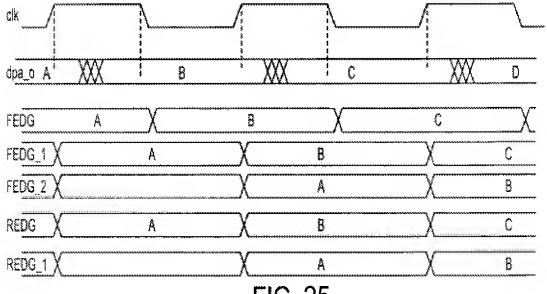

FIG. 25

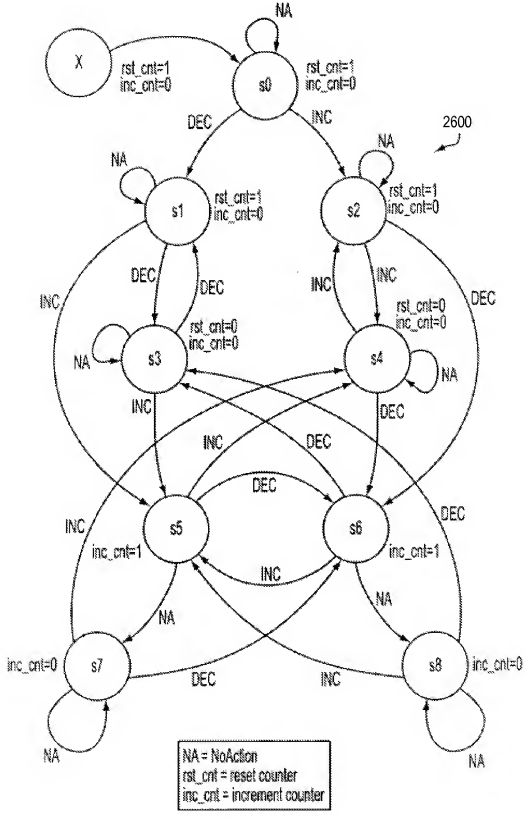
X
rst_cnt=1
inc_cnt=0
NA
s0
rst_cnt=1
inc_cnt=0
DEC
INC
2600
s1
rst_cnt=1
inc_cnt=0
s2
rst_cnt=1
inc_cnt=0
s3
rst_cnt=0
inc_cnt=0
s4
rst_cnt=0
inc_cnt=0
s5
inc_cnt=1
s6
inc_cnt=1
s7
inc_cnt=0
s8
inc_cnt=0
NA = NoAction
rst_cnt = reset counter
inc_cnt = increment counter

FIG. 26

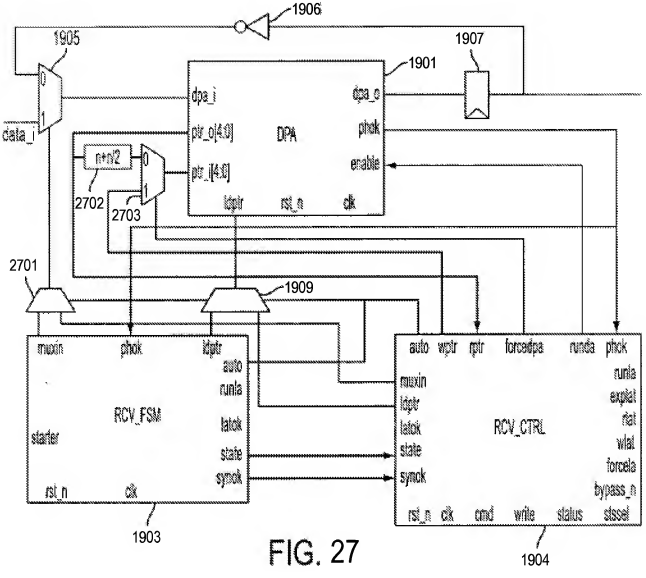
1906
1905
1907
1901
dpa_i
dpa_o
data_i
ptr_o[4:0]
DPA
phok
n+n/2
ptr_i[4:0]
enable
2702
2703
ldptr
rst_n
clk
2701
1909
muxin
phok
ldptr
auto
runla
RCV_FSM
latok
starter
state
synok
rst_n
clk
1903
auto
wptr
rptr
forcedpa
runda
phok
runla
muxin
expist
ldptr
rist
latok
RCV_CTRL
wist
state
forcela
synok
bypass_n
rst_n
clk
cmd
write
status
sissel
1904

FIG. 27

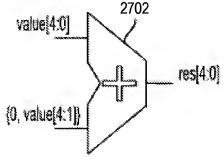
2702
value[4:0]
res[4:0]
{0, value[4:1]}

FIG. 28

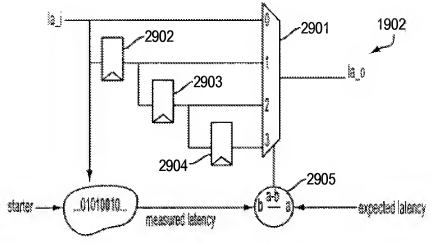
la_i
2902
2901
1902
la_o
2903
2904
2905
starter
...01010010...
measured latency
expected latency

FIG. 29

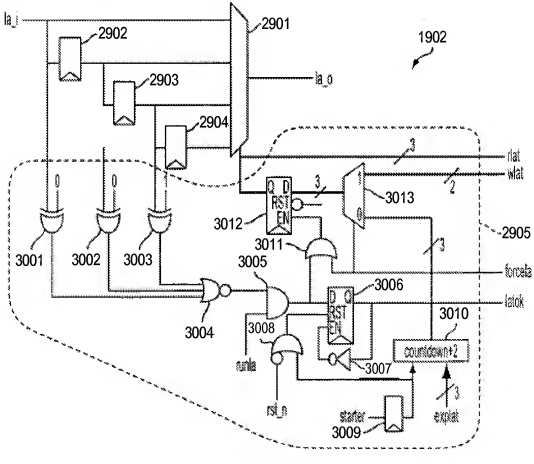
la_i
2902
2901
1902
la_o
2903
2904
rlat
wlat
3013
2905
3012
3011
3001
3002
3003
3005
forcela
3006
latok
3004
3008
3010
countdown+2
3007
sunla
rsl_o
starter
3009
expla

FIG. 30

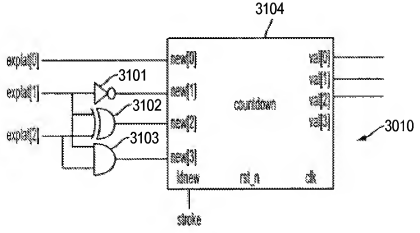
3104
explat[0]
explat[1]
explat[2]
3101
3102
3103
new[0]
new[1]
new[2]
new[3]
countdown
va[0]
va[1]
va[2]
va[3]
3010
ldnew
rst_n
clk
stroke

FIG. 31

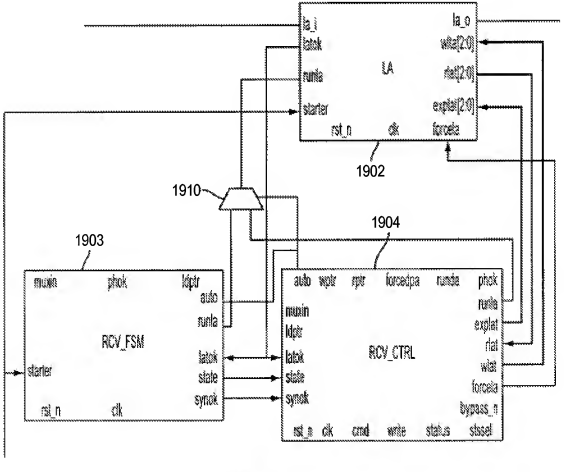
la_i
latok
runla
starter
rst_n
clk
LA
la_o
wlat[2:0]
rlat[2:0]
explat[2:0]
forcela
1902
1910
1904
1903
muxin
phok
ldptr
auto
runla
RCV_FSM
latok
starter
state
synok
rst_n
clk
auto
wptr
rptr
forcedpa
runde
phok
runla
muxin
explat
ldptr
rlat
RCV_CTRL
latok
wlat
state
forcela
synok
bypass_n
rst_n
clk
cmd
write
status
stsset

FIG. 32

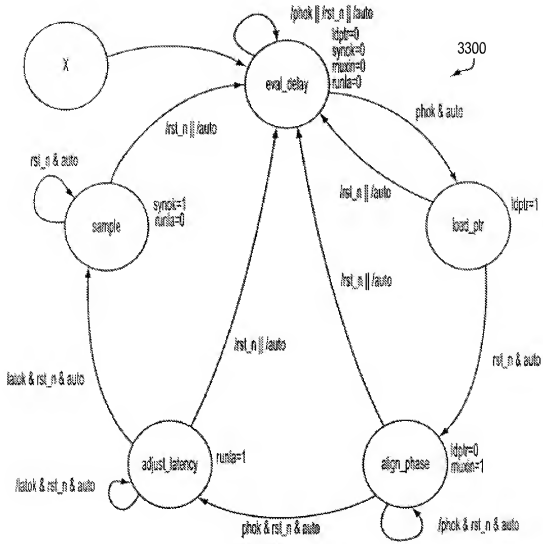

FIG. 33

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WSXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO

FIG. 34

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
XXXXXXXXXX		SYNOK	LATOK	PHOK	FSM_STATE			RLAT			RPTR				

FIG. 35

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

FIG. 36

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
1	X	0	EXPECTED LATENCY			X	0	X	X	X	X	X	X	X	1

FIG. 37

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
1	0	0	X	X	X	0	1	1	0	0	0	0	0	0	0

FIG. 38

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
1	0	0	X	X	X	1	0	0	0	0	0	0	0	0	0

FIG. 39

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
1	0	0	X	X	X	0	0	1	X	X	X	X	X	1	0

FIG. 40

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
1	0	0	X	X	X	1	0	0	X	X	X	X	X	0	0

FIG. 41

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
1	1	0	EXPECTED LATENCY			1	0	0	X	X	X	X	X	0	0

FIG. 42

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
1	0	0	X	X	X	1	0	0	X	X	X	X	X	0	0

FIG. 43

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
BP_N	RLA	FLA	WEXPLAT			RDPA	FDPA	LPTR	WPTR					MUXIN	AUTO
1	1	0	1	1	1	1	0	0	X	X	X	X	X	0	0

FIG. 44